Smruti Ranjan Sarangi

CONTACT INFORMATION

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CURRENT POSITION

I am currently employed as an Associate professor (and Usha Hasteer Chair Professor) in the Computer Science and Engineering Department at IIT Delhi. I hold a joint appointment with the Department of Electrical Engineering and I am associated with the School of Information Technology and the Bharti School of Telecommunication. I teach courses and conduct research in computer architecture, operating systems, parallel and distributed systems.

RESEARCH INTERESTS

Computer Architecture(Primary Interest): Reliability, Hardware support for operating systems, Optical networking, Temperature modeling.
Architectures for machine learning: CNNs, RNNs, GANs, and customized solutions for drones and AR devices.
Parallel Algorithms: Non-blocking data structures, Wait-free slot schedulers
Operating Systems: Jitter free operating systems, HW/SW codesign of operating systems
Total Research Contribution: 30 Journal papers, 62 Conference papers, 5 US Patents + 5 Indian patents filed, 2 best paper awards + 2 nominations, 8.5 crores (1 crore Indian rupees is 150K USD) of research funding (as PI)

EDUCATION

University of Illinois at Urbana-Champaign, IL(UIUC)

Ph.D., Computer Science, May 2007 (GPA 3.95/4.00)
Thesis Title: Techniques to Mitigate the Effects of Congenital Faults in Processors
Advisor: Josep Torrellas

University of Illinois at Urbana Champaign, IL(UIUC)

M.S., Computer Science, Dec, 2004 (GPA 3.95/4.00)

Indian Institute of Technology, Kharagpur, India

B.Tech, Computer Science, May 2002 (GPA 9.33/10.00)

EMPLOYMENT

Computer Science and Engg. Deptt., IIT Delhi

Associate Professor (Jan 2017 till date)

Computer Science and Engg. Deptt., IIT Delhi

Assistant Professor (Jan 2011 till Jan 2017)

IBM Research Labs, Bangalore

Research Staff Member (April 2009 till Jan 2011)

India Systems and Technology Labs, IBM, Bangalore

Advisory Research Engineer (Nov 2007 till March 2009)

Synopsys Research, Bangalore

Researcher (Feb 2007 to Oct 2007)

Books

[**Textbook**] Computer Organisation and Architecture by Smruti R. Sarangi, 688 pages, McGrawHill, 2014.

[**Reference Book**] Techniques to Mitigate the Effects of Congenital Faults in Processors by Smruti R. Sarangi and Josep Torrellas 160 pages, ISBN: 978-3-639-04637-3, VDM Verlag, 2008. (based on Ph.D thesis)

Honors and Awards

Papers nominated for the best paper award: ICCAD 2019 and ASPDAC 2016.

Usha Hasteer Chair Professorship, IIT Delhi, 2019-24

Visvesvaraya Young Faculty Fellowship, 2014-15, by the Ministry of IT and Telecommunications, Government of India.

Best paper award received at the Security and Privacy Symposium for the paper, "Ethical Hacking of License Managers." (2015)

Teaching excellence award, best undergraduate teacher in the large class category, 2014.

Nucleus group young faculty award (IIT Delhi), 2011.

IBM Chairman's Equity Award (Top 1% in every unit), Nov 17, 2008.

Recognized as IBM Top Talent(Top 10% in every unit) since June 2008.

"Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware", selected in IEEE Micro Top picks. (top 13 papers in computer architecture in 2006)

"Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware", **Best Paper Award, MICRO 2006**

"Energy-Efficient Thread-Level Speculation on a CMP" selected in IEEE Micro Top picks. (top 13 papers in computer architecture in 2005)

David J. Kuck, Best MS thesis award in the department of computer science, UIUC in 2004.

Professional Service

Member of the program committees of HiPC, IPDPS, ICDCIT, VLSID, ICCD **2013-19**

Student Symposium Chair: HiPC	**Dec. 2010**
Program Committee Member: HiPC	**Dec. 2010**
Workshop Chair : Cloud Computing held along with HIPC	**Dec. 2009**
Workshop/Tutorials Chair for PPoPP	**Dec. 2009**
Registration chair for HPCA	**Dec. 2009**
Student Research Co-ordinator for HiPC	**Dec. 2009**
Program Committee member for NISS, NCM, ICCIT	**2009**

Reviewed papers for HPCA, MICRO, ISCA, OSDI, ASPLOS, PPopp, PLDI, HiPC, CGO, PODC, DSN, HiPC, IPDPS, DAC, ACM TACO, IEEE TPDS.

Teaching Experience

Courses taught at IIT Delhi (2000+ students): Advanced Distributed Systems, Principles of Multiprocessor Systems, Computer Architecture, Fault Tolerant Systems, Architecture of High Performance Computers, Introduction to Programming.

Teaching Outreach activity:

1. Co-chaired a committee to design a new curriculum for schools. A novel curriculum was designed with emphasis on computational thinking. This was adopted by the CBSE board, and has was made operational on Apr 1, 2018.
2. Taught 3 NPTEL courses on computer architecture.
3. Conducted workshops for school children preparing for the international informatics olympiad at IIIT Delhi. (2014 and 2015)
4. Taught the computer architecture course at IIT Ropar for 2 years (via video) (2011 and 2012).
5. Taught a remote course for students at the Addis Abbaba university, Ethiopia. (2011)

Publications

International Journal Papers

1. A Formal Approach to Accountability in Heterogeneous Systems-on-chip, Rajshekar Kalayappan and Smruti R. Sarangi, IEEE Transactions on Dependable and Secure Computing (IEEE TDSC), (accepted) Impact factor: 6.4
2. ChunkedTejas: A Chunking-based Approach to Parallelizing a Trace-Driven Architectural Simulator, Rajshekar Kalayappan, Smruti R. Sarangi, ACM Transactions on Modeling and Computer Simulation (TOMACS), (accepted) Impact factor: 0.54
3. Predict, Share, and Recycle your Way to Low Power Nanophotonic Networks, Janibul Bashir, Smruti R. Sarangi. ACM Journal on Emerging Technologies in Computing Systems (ACM JETC), Volume 16, Issue 1, Article No. 4, October 2019. Impact factor: 1.47
4. SpliESR: Tunable Power Splitter based on an Electro-Optic Slotted Ring Resonator, Rajib R. Ghosh, Janibul Bashir, Smruti R. Sarangi, Anuj Dhawan, Optics Communications, vol: 442, pages 117-122, July 2019. Impact factor: 1.89
5. Enhancing Network-on-Chip Performance by Reusing Trace Buffers by Neetu Jindal, Shubhani Gupta, Divya Praneetha, Preeti Ranjan Panda, Smruti R. Sarangi, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), April 2020, Volume 39, Issue 4, pages: 922–935, Impact factor: 1.2
6. A Survey of Chip Level Thermal Simulators by Hameedah Sultan, Anjali Chauhan, and Smruti R. Sarangi, ACM Computing Surveys, Volume 52, Issue 2, Article No. 42, April 2019. Impact factor: 6.13
7. BigBus: A Scalable Optical Interconnect, Janibul Bashir, Eldhose Peter, and Smruti R. Sarangi. ACM Journal of Emerging Technologies in Computing Systems (ACM JETC), Volume 15, No. 1, Article No. 8, Jan 2019. Impact factor: 1.47
8. A Survey of On-chip Optical Interconnects, Janibul Bashir, Eldhose Peter, and Smruti R. Sarangi. ACM Computing Surveys, Volume 51, No. 6, Article No. 115, Jan 2019. Impact factor: 6.13
9. Radio Propagation Characteristics-Based Spoofing Attack Prevention on Wireless Connected Devices by Mihiro Sonoyama, Takatsugu Ono, Haruichi Kanaya, Osamu Muta, Smruti R. Sarangi, Koji Inoue, Journal of Information Processing, Volume 27, pages: 322-334, Jan 2019. SJR Rank: 0.26.
10. Providing Accountability in Heterogeneous Systems On-Chip by Rajshekar Kalayappan and Smruti R. Sarangi, ACM Transactions on Embedded Computing Systems, Volume 17, No. 5, Article No. 83, Sept 2018. Impact factor: 1.37
11. Task Assignment Algorithms for Multicore Platforms with Process Variations, Gayathri Ananthanarayanan, Smruti R. Sarangi, M. Balakrishnan, Journal of Low Power Electronics (JOLPE), Volume 14, Issue 2, June 2018, Pages 302 – 317. Impact factor: 1.22
12. Reusing Trace Buffers as Victim Caches, Neetu Jindal, Smruti R. Sarangi, Preeti Panda, IEEE Transactions on VLSI, Volume 26, Issue 9, September 2018, pages: 1699 – 1712. Impact factor: 1.95

13. ParTejas: A Parallel Simulator for Multicore Processors by Geetika Malhotra, Rajshekar Kalayappan, Seep Goel, Pooja Aggarwal, Abhishek Sagar, and Smruti R. Sarangi. ACM Transactions on Modeling and Computer Simulation. (ACM TOMACS), Volume 27, No. 3, Article 19, July 2017. Impact factor: 0.54
14. Managing Trace Summaries to Minimize Stalls During Post-Silicon Validation by Sandeep Chandran, Preeti Panda, Smruti R. Sarangi, Ayan Bhattacharya, Deepak Chauhan, Sharad Kumar, IEEE Transactions on VLSI, Volume 25, Issue 6, June 2017, pages: 1881-1894. Impact factor: 1.95
15. Optical Overlay NUCA: A High Speed Substrate for Shared L2 Caches, by Eldhose Peter, Anuj Arora, Janibul Bashir, Akriti Bagaria, and Smruti R. Sarangi. ACM Journal on Emerging Technologies in Computing Systems. ACM Journal on Emerging Technologies in Computing Systems (JETC), Volume 13, Issue 4, May 2017, pages: 1-25. Impact factor: 1.47
16. Internet of Things: Architectures, Protocols, and Applications by Pallavi Sethi, and Smruti R. Sarangi. Journal of Electrical and Computer Engineering. Volume 2017. SJR Rank: 0.22
17. FluidCheck: A Redundant Threading based Approach for Reliable Execution in Manycore Processors, Rajshekar Kalayappan, and Smruti R. Sarangi. ACM Transactions on Architecture and Code Optimization (TACO). Volume 12 Issue 4, January 2016. Also presented at the European Network on High Performance and Embedded Architecture and Compilation Conference (HiPEAC) 2016, Prague. Impact factor: 1.63.
18. Active Microring Based Tunable Optical Power Splitters, Eldhose Peter, Arun Thomas, Anuj Dhawan, Smruti R. Sarangi. Optics Communications, Volume 359, Pages 311 – 315, 2016. Impact factor: 1.89.
19. Area-aware Cache Update Trackers for Post-silicon Validation, Sandeep Chandran, Smruti R. Sarangi, Preeti Panda, IEEE Transactions on VLSI Systems, Volume 24, Issue 5, May 2016, pages: 1794-1807. Impact factor: 1.95
20. Lock-free and Wait-free Slot Scheduling Algorithms by Pooja Aggarwal and Smruti R. Sarangi, IEEE Transactions on Parallel and Distributed Systems, Volume 27, Issue 5, Pages: 1387-1400, 2016. Impact factor: 3.4.
21. FP-NUCA: A Fast NOC Layer for Implementing Large NUCA Caches, Anuj Arora, Mayur Harne, Hameedah Sultan, Akriti Bagaria, Smruti R. Sarangi. IEEE Transactions on Parallel and Distributed Systems. Volume: 26, Issue: 9 Pages: 2465 - 2478, 2015. Impact factor: 3.4.
22. Processor Power Estimation Techniques: A Survey, Hameedah Sultan, Gayathri Ananthanarayanan, and Smruti R. Sarangi. International Journal of High Performance Systems Architecture. Volume 5 Issue 2, May 2014, Pages 93-114. SJR Rank: 0.12
23. Architectural Support for Handling Jitter in Shared Memory based Parallel Applications by Sandeep Chandra, Prathmesh Kallurkar, Parul Gupta, Smruti R. Sarangi, IEEE Transactions on Parallel and Distributed Systems. Volume 25, Issue 5, Pages: 1166-1176, May 2014. Impact factor: 3.4.
24. Amdahl's Law in the Era of Process Variation by Gayathri Ananthanarayanan, Geetika Malhotra, M. Balakrishnan, and Smruti R. Sarangi. International Journal of High Performance Systems Architecture (IJHPSA). 2013, Vol 4, No. 4. pp 218-230. SJR Rank: 0.12

25. A Survey of Checker Architectures by Rajshekar Kalayappan and Smruti R. Sarangi, ACM Computing Surveys, Volume 45, Issue 4, Number 48, 2013. Impact factor: 6.13
26. IT Infrastructure for Providing Energy-as-a-Service to Electric Vehicles by Smruti R. Sarangi, Partha Dutta, and Komal Jalan in IEEE Transactions on Smart Grids. Impact factor: 10.49 Vol. 3, Issue 2, pages 594-604, 2012.
27. VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects by Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, IEEE Transactions on Semiconductor Manufacturing (IEEE TSM), February 2008. Volume 21, Issue 1, pp 3–13. Impact factor: 1.34
28. Patching Processor Design Errors with Programmable Hardware, Smruti R. Sarangi, Satish Naraya- naswamy, Bruce Carneal, Abhishek Tiwari, Brad Calder, Josep Torrellas. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture, Jan. 2007, Volume 27, Issue 1, pages 12–25. Impact factor: 1.91
29. Energy-Efficient Thread-Level Speculation on a CMP by Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti R. Sarangi, James Tuck and Josep Torrellas. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture, Jan. 2006, Volume 26, Issue 1, pages 80–91. Impact factor: 1.91
30. A Scalable Efficient and General Monte Carlo Scheme for Generating Synthetic Web Request Streams by Smruti R. Sarangi, P.N.Sireesh and S.P.Pal. International Journal of Computer Systems Science and Engineering, Vol. 18, pp, 121-128, May 2003. SJR Rank: 0.22

Conference Papers

1. Softmon: A Tool to Compare Similar Open-source Software from a Performance Perspective, Shubhankar Suman Singh and Smruti R. Sarangi, Mining Software Repositories (MSR), Seoul (accepted)
2. VarSim: A Fast and Accurate Variability and Leakage Aware Thermal Simulator, Hameedah Sultan, Smruti R. Sarangi. Design Automation Conference (DAC), San Francisco (accepted)
3. Performance Prediction for Multi-Application Concurrency on GPUs, Diksha Moolchandani, Sudhanshu Gupta, Anshul Kumar, Smruti R. Sarangi, International Symposium on Performance Analysis of Systems and Software (ISPASS), Boston, USA. (accepted)
4. Power efficient Photonic Network-on-Chip for a Scalable GPU, Janibul Bashir, Khushal Sethi and Smruti R. Sarangi. International Symposium on Networks-on-Chip (NOCS), New York, 2019.
5. NanoTherm: An Analytical Fourier-Boltzmann Framework for Full Chip Thermal Simulations, Shashank Varshney, Hameedah Sultan, Palkesh Jain, Smruti R. Sarangi. International Conference on Computer Aided Design (ICCAD), Westminister, USA, 2019. **Nominated for the best paper award**
6. F-LaaS: A Control-Flow-Attack Immune License-as-a-Service Model, Sandeep Kumar, Diksha Moolchandani, Takatsugu Ono and Smruti Sarangi.IEEE Services Computing Conference (SCC), 2019. Milan, Italy, 2019.

7. A Reference Architecture for Smart and Software-defined Buildings, Manuel Mazzara, Ilya Afanasyev, Smruti R. Sarangi, Salvatore Distefano, Vivek Kumar, Muhammad Ahmad, International Workshop on Sensors and Smart Cities (part of IEEE SmartComp), Washington DC, 2019.
8. FlexiCheck: An Adaptive Checkpointing Architecture for Energy Harvesting Devices, Priyanka Singla, Shubhankar Suman Singh, and Smruti R. Sarangi. Design Automation and Test in Europe, (DATE), Florence, Italy, 2019.
9. Slotted Electro-optic Ring Resonator as a Tunable Optical Power Splitter, Rajib R. Ghosh, Janib Bashir, Smruti R. Sarangi, Anuj Dhawan, SPIE Photonics West, OPTO, Silicon Photonics XIV, San Francisco, USA, 2019.
10. Probabilistic Sequential Consistency in Social Networks, Priyanka Singla, Shubhankar Suman Singh, K. Gopinath, and Smruti R. Sarangi, HiPC (High Performance Computing), Bangalore, India, 2018.
11. Whitelisting Approach Using Hardware Performance Counters in IoT Microprocessors, Ghadeer Alumsaddar, Teruo Tanimoto, Takatsugu Ono, Smruti R. Sarangi, and Koji Inoue, Career Workshop for Women and Minorities in Computer Architecture (CWWMC, held along with MICRO) 2018
12. Energy Efficient Scheduling in IoT Networks, Smruti R. Sarangi, Sakshi Goel and Bhumika Singh, ACM Symposium on Applied Computing (SAC), Pau, France, 2019.
13. HPXA: A Highly Parallel XML Parser, Isaar Ahmad, Sanjog Patil, and Smruti R. Sarangi, DATE (Design Automation and Test in Europe), Dresden, Germany, 2018.
14. Expander: Lock-Free Cache for a Concurrent Data Structure, Pooja Aggarwal, Smruti R. Sarangi, HiPC (High Performance Computing), Jaipur, India, 2017.
15. NUPLet: A Photonics Based Multi-Chip NUCA Architecture, Janibul Bashir, Smruti R. Sarangi, ICCD (International Conference on Computer Design), Boston, USA, 2017.
16. SchedTask: A Hardware-Assisted Task Scheduler, Prathmesh Kallurkar, Smruti R. Sarangi, MICRO (International Symposium on Microarchitecture), Boston, USA, 2017.
17. BigBus: A Scalable Optical Interconnect by Eldhose Peter, Janib-ul Bashir, and Smruti R. Sarangi. PACT (Parallel Architectures and Compilation Techniques), Portland, USA, 2017.
18. Reusing Trace Buffers to Enhance Cache Performance, Neetu Jindal, Preeti R. Panda, and Smruti R. Sarangi. DATE (Design Automation and Test in Europe), Lausanne, Switzerland, 2017.
19. A Hardware Implementation of the MCAS Synchronization Primitive, Sristhy Patel, Rajshekar Kalayappan, Ishani Mahajan, and Smruti R. Sarangi. DATE (Design Automation and Test in Europe), Lausanne, Switzerland, 2017.
20. A Fast Leakage Aware Simulator for 3D Chips, Hameedah Sultan, and Smruti R. Sarangi, DATE (Design Automation and Test in Europe), Lausanne, Switzerland, 2017.
21. pTask: A Smart Prefetching Scheme for OS Intensive Applications, Prathmesh Kallurkar, Smruti R. Sarangi, International Symposium on Microarchitecture (MICRO), Taipei, Taiwan, 2016.

22. Leakage Power Aware Task Assignment Algorithms for Multicore Platforms, Gayathri Ananthanarayanan, Smruti R. Sarangi, M. Balakrishnan, International Annual Symposium on VLSI (ISVLSI), Pittsburgh, USA, 2016.
23. SecCheck: A Trustworthy System with Untrusted Components, Rajshekar Kalayappan, Smruti R. Sarangi, International Annual Symposium on VLSI (ISVLSI), Pittsburgh, USA, 2016.
24. Noise Aware Scheduling in Data Centers, Hameedah Sultan, Arpit Katiyar, Smruti R. Sarangi. International Conference on Supercomputing (ICS), 2016. Istanbul (accepted)
25. OptiShare: A Dynamic Channel Sharing Scheme for Power Efficient On-chip Optical Architectures, Eldhose Peter, Smruti R. Sarangi, OPTICS workshop, along with Design Automation and Test in Europe (DATE) 2016, Dresden, Germany
26. A Wait-Free Stack, Seep Goel, Pooja Aggarwal, Smruti R. Sarangi, International Conference on Distributed Computing and Internet Technology (ICDCIT), Bhubaneshwar, 2016
27. A Generic Implementation of Barriers using Optical Interconnects, Sandeep Chandran, Eldhose Peter, Preeti R. Panda, Smruti R. Sarangi, VLSI Design, Kolkata, 2016
28. Extending Trace History Through Tapered Summaries in Post-silicon Validation, Sandeep Chandran, Preeti Ranjan Panda, Smruti R. Sarangi, Deepak Chauhan, Sharad Kumar, Asia and South Pacific Design Automation Conference (ASPDAC), Macao, 2016. **(Nominated for the Best Paper Award)**
29. ColdBus: A Near-Optimal Power Efficient Optical Bus, Eldhose Peter, Arun Thomas, Anuj Dhawan, Smruti R. Sarangi, HiPC (High Performance Computing), Bangalore, 2015.
30. Tejas: A Java based Versatile Micro-architectural Simulator, Smruti R. Sarangi, Rajshekar Kalayappan, Prathmesh Kallurkar, Seep Goel, Eldhose Peter. PATMOS, Salvador Brazil, 2015.
31. SecX: A Framework for Collecting Runtime Statistics for SoCs with Multiple Accelerators, Rajshekar Kalayappan and Smruti R. Sarangi, ISVLSI, Montpeller, France, 2015
32. Ethical Hacking of License Managers, Karishma Agarwal, Prathmesh Kallurkar, Siva Krishna Aleti, Smruti R. Sarangi. Security and Privacy Symposium, IIIT Delhi, 2015 **(Best Paper Award)**.
33. Optimal Power Efficient Photonic SWMR Buses, Eldhose Peter, Smruti R. Sarangi, 2nd Workshop on Silicon Photonics, along with the HiPEAC Conference, Amsterdam, 2015.
34. RADIR: Lock-free and Wait-free Bandwidth Allocation Models for Solid State Drives, Pooja Aggarwal, Giridhar Yasa, Smruti R. Sarangi, HiPC, Goa, 2014.
35. Optical Overlay NUCA: A High Speed Substrate for Shared L2 Caches, Eldhose Peter, Anuj Arora, Akriti Bagaria, Smruti R. Sarangi, HiPC, Goa, 2014.
36. Trikon: A Hypervisor Aware Manycore Processor, Rohan Bhalla, Prathmesh Kallurkar, Nitin Gupta, Smruti R. Sarangi, HiPC, Goa, 2014.
37. GPUTejas: A Parallel Simulator for GPU Architectures, Geetika Malhotra, Seep Goel, Smruti R. Sarangi, HiPC, Goa, 2014.

38. ParTejas: A Parallel Simulator for Multicore Processors, Geetika Malhotra, Pooja Aggarwal, Abhishek Sagar, Smruti R. Sarangi. ISPASS, Monterey, CA, US, 2014.
39. Software Transactional Memory Friendly Slot Schedulers by Pooja Aggarwal, and Smruti R. Sarangi, ICDCIT, Bhubaneswar, 2014.
40. OptiKit: An Open Source Kit for Simulation of On-Chip Optical Components by Eldhose Peter, and Smruti R. Sarangi. VLSI Design (Poster), Mumbai, 2014.
41. LightSim : A Leakage Aware Ultrafast Temperature Simulator by Smruti R. Sarangi, Gayathri Ananthanarayanan, and M. Balakrishnan, ASP-DAC, Singapore, 2014.
42. A Case Study of a First-of-Its-Kind Remote Course among Premier Institutions in India by Smruti R. Sarangi, International Conference on E-Learning and E-Technologies in Education, (ICEEE), Lodz, Poland, 2013.
43. emuArm: A Tool for Teaching the ARM Assembly Language by Geetika Malhotra, Namita Atri, Smruti R. Sarangi, International Conference on E-Learning and E-Technologies in Education, (ICEEE), Lodz, Poland, 2013.
44. Space Sensitive Cache Dumping for Post Silicon Validation by Sandeep Chandran, Smruti R. Sarangi, Preeti Ranjan Panda, Design Automation and Test in Europe (DATE), Grenoble, France, 2013.
45. Lock-free and Wait-free Slot Scheduling Algorithms by Pooja Aggarwal, Smruti R. Sarangi, International Parallel and Distributed Processing Symposium (IPDPS), Boston, USA, 2013.
46. Efficient on-line algorithms for maintaining k-cover of a sparse bit-string by Amit Kumar, Preeti Panda, Smruti R. Sarangi, Foundations of Software Technology and Theoretical Computer Science (FSTTCS), Hyderabad, India, 2012.
47. UsiFe: An User Space Filesystem with Support for Intra File Encryption by Rohan Sharma, Prathmesh Kallurkar, Saurabh Kumar, and Smruti R. Sarangi, International Conference on Software and Computing Technology (ICSCT), Singapore, 2011.
48. Virtualized Base Station Pool : Towards a Wireless Network Cloud for Radio Access Networks by Zhenbo Zhu, Qing Wang, Yonghua Lin, Parul Gupta, Smruti R. Sarangi Shivkumar Kalyanaraman, Hubertus Franke. ACM Computing Frontiers, Italy, 2011.
49. DUST: A Generalized Notion of Similarity between Uncertain Time Series by Smruti R. Sarangi, and Karin Murthy.Knowledge Discovery and Data Mining(KDD), Washington D.C., USA, 2010.
50. Theoretical Framework for Eliminating Redundancy in Workflows by Dhrubajyoti Saha, Abhishek Samanta, and Smruti R. Sarangi. IEEE International Conference on Service Computing (SCC), Bangalore, September 2009.
51. High Performance SWR Base Station and Wireless Network Cloud over General Multicore IT Platforms by Yonghua Lin, Qing Wang, Zhenbo Zhu, Jianwen Chen, Lin Chen, Rong Yan, Wei Xie, Kuan Feng, Parul Gupta, Smruti R. Sarangi (demo paper) in MobiCom, Beijing, 2009.
52. EVAL: Utilizing Processors with Variation-Induced Timing Errors by Smruti Sarangi, Brian Greskamp, Abhishek Tiwari, and Josep Torrellas. 41st International Symposium on Microarchitecture (MICRO), Lake Como, Italy, November 2008.
53. VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects by Radu Teodorescu, Brian Greskamp, Jun Nakano, Smruti Sarangi, Abhishek

Tiwari, and Josep Torrellas (UIUC). 2nd Workshop on Architectural Support for Gigascale Integration (ASGI) (along with ISCA 2007), San Diego, USA, June 2007.

54. ReCycle: Pipeline Adaptation to Tolerate Process Variation by Abhishek Tiwari, Smruti Sarangi, and Josep Torrellas, 34th Annual International Symposium on Computer Architecture (ISCA), San Diego, USA, June 2007.
55. Threshold Voltage Variation Effects on Aging-Related Hard Failure Rates by Brian Greskamp, Smruti Sarangi, and Josep Torrellas. International Symposium on Circuits and Systems (ISCAS), Special Session: Circuit Design in the Presence of Device Variability, Taipei, May 2007.
56. A Model for Timing Errors in Processors with Parameter Variation by Smruti Sarangi, Brian Greskamp, and Josep Torrellas. 8th International Symposium on Quality Electronic Design (ISQED), March 2007.
57. Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware by Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas. 39th International Symposium on Microarchitecture (MICRO), Dec. 2006. **(Best Paper Award)**
58. Designing Hardware that Supports Cycle-Accurate Deterministic Replay by Brian Greskamp, Smruti R. Sarangi and Josep Torrellas. Workshop on Complexity Effective Design(WCED) (along with ISCA 2006).
59. Rapid Prototyping in Architecture Research using Existing Hardware Mechanisms by Smruti R. Sarangi, Brian Greskamp and Josep Torrellas. Workshop on Architectural Research Prototyping(WARP) (along with ISCA 2006).
60. Cycle-Accurate Deterministic Replay for Processor Debugging by Smruti R. Sarangi Brian Greskamp and Josep Torrellas. Dependable Systems and Networks (DSN) 2006.
61. ReSlice: Selective Re-Execution of Long-Retired Misspeculated Instructions Using Forward Slicing by Smruti R. Sarangi, Wei Liu, Josep Torrellas, and Yuanyuan Zhou. 38th International Symposium on Microarchitecture (MICRO), November 2005.
62. Thread-Level Speculation on a CMP Can Be Energy Efficient by Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. 2005 ACM International Conference on Supercomputing (ICS), June 2005.

Patents Filed

1. Process and System for Using Unused Optical Power in Photonic On-Chip Networks, Janibul Bashir, Smruti R. Sarangi. Filed at the Indian patent office. Date: 18/02/2020. Number: 202011006878
2. A Graphics Processor Unit (GPU) System with Photonics based On-chip Network, Janibul Bashir, Smruti R. Sarangi. Filed at the Indian Patent office Date: November 19th, 2019. Number: 201911047168
3. System and method for improving the performance of an architectural simulator, Rajshekar Kalayappan, Avantika Chhabra, Smruti R. Sarangi, IIT Delhi. Filed at the Indian Patent Office. Date: 17th April 2018, Number: 201811014613
4. A System-on-Chip with In-Built Mechanism and method for Identification of Faulty Components in the System-on-Chip, Rajshekar Kalayappan, Smruti R. Sarangi, IIT Delhi. Filed at the Indian Patent Office. Date: 20 Feb. 2018. Number: 201811006458
5. Energy Efficient Scheduling of tasks in an IoT Network, Smruti R. Sarangi, Sakshi Goel, Bhumika Singh, IIT Delhi. Filed at the Indian Patent Office. Date: 5th Jan 2017. Number: 201711000557
6. Systems and methods for exploring and utilizing solutions to cyber-physical issues in a sandbox, Ullas Nambiar, Smruti R. Sarangi, Biplav Srivastava, Vivek Tyagi, IBM Corp. US PTO Number: US 13/088,915
7. Distributed symbol table with intelligent lookup scheme, Sikta Pany, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/717,601
8. Optimizing Workflow Engines, Dhrubajyoti Saha, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/726,798
9. Accelerating Generic Loop Iterators Using Speculative Execution, Ganesh Bikshandi, Dibyendu Das, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/938,312
10. Generalized notion of similarities between uncertain time series, Karin Murthy, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/833,055

Research Projects

S. No.	Title	Cost	Duration	Agency
as PI				
13	Book Writing Grant	1.77 lakhs	2020-25	Qualcomm
12	Book Writing Grant	1.77 lakhs	2020-25	Intel
11	Book Writing Grant	70,000	2020-25	AMD
10	Design of Energy Efficient Computing Systems for Mobile Vision Applications	38 lakhs	2019-22	Ministry of Science and Technology
9	Smart Infrastructure for an Electric Vehicle Ecosystem	6.5 crores	2018-23	Ministry of HRD and IIT Delhi
8	Ultra-Fast Thermal Simulation of Electronic Systems	30,000 (USD)	2017-20	Semiconductor Research Corporation, USA
7	Support for Secure Execution in Distributed Systems using Encrypted Keys	30,000 (USD)	2017-20	Semiconductor Research Corporation, USA
6	Characterization of Operating Systems for System Intensive Workloads	12.5 lakhs	2015-17	Netapp India Pvt. Ltd.
5	Design of Energy Efficient Optical Networks in Multicore Processors	33 lakhs	2014-17	Ministry of Science and Technology
4	Lock Free Algorithms for Scheduling in Storage Systems	13 lakhs	2013-14	Netapp India Pvt. Ltd.
3	BhartiSim: An Advanced Micro-architectural Simulator	61 lakhs	2012-15	Ministry of IT
2	Temperature Aware Placement in Large Multicore Processors, Planning	10 lakhs	2011-13	IIT Delhi
1	Process Variation aware Computer Architecture	1 lakh	2011-12	IIT Delhi
as co-PI				
6	Research and development of smart, secure, scalable, resilient and adaptive cyber-physical power system	3 crores	2018-21	Ministry of Science and Technology
5	Security of Connected Devices in 5G	95 lakhs	2018-20	Department of Telecommunications
4	Security in the Internet of Things Space	1.44 crores	2017-22	Ministry of Science and Technology and JST (Japan)
3	Advanced Debug Architecture and Methodology for Heterogeneous Multicore Platforms	32 lakhs	2014-17	Semiconductor Research Corporation
2	Structured Sharing of Networks and Computer Resources in a Community of Devices	200k USD	2013-20	Intel, USA
1	Characterization of Multi-core Processors for Power-Estimation at System-Level	15.5 lakhs	2011-13	Ministry of Science and Technology
1 lakh → 100,000, 1 crore → 10 million				