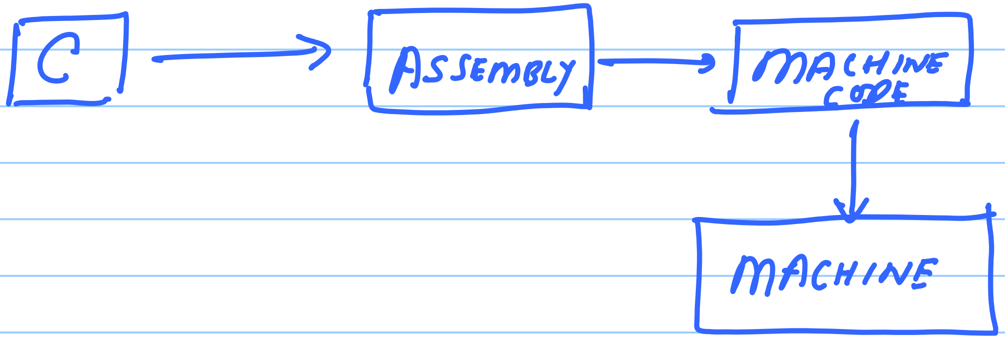
Sept-18

4) Design of the processor.



ARM & MIPS : Reduced Inst. Sets. (RISC)

X86 ' CISC - Complex Inst. Set

mips

→ 32 Registers

→ r_0 → (zero reg.) (hardwired to 0)

→ r_{29} → stack ptr.

→ r_{31} → lr

(No PC and CPSR)

OPcodes.

add	$\$r_2, \$r_3, \$r_4$	$r_2 = r_3 + r_4$
sub	$\$r_2, \$r_3, \$r_4$	$r_2 = r_3 - r_4$
addi	$\$r_2, \$r_3;\ 30$	$r_2 = r_3 + 30$

R-format insts. (add, sub)

6	5	5	5	5	6
opcode	r_s	r_t	r_d	shift	func.

lw $\$r_2$, 20($\$r_3$)

sw $\$r_2$, 20($\$r_4$)

I-format insts. (addi, lw, sw)

6	5	5	16
opcode	r_s	r_t	offset/immediate
	base reg.	dest.	

Immediate is 16 bits (2 bytes)

🚩 Very convenient.

How do you load a 32 bit constant into a register).

0x FFFD EA 09

add $\$r_2$, $\$r_0$, 0xEA09

lui $\$r_2$, 0xFFFD

shift left logical: sll.

shift right logical: srl

Branches

beq $\$r_2$, $\$r_3$, 25 (if ($r_2 == r_3$)
(bne) pc += 4 + 100)

Jump.

j 25 go to 100 (absolute)

jr $\$r_{31}$ (same as pc = lr)

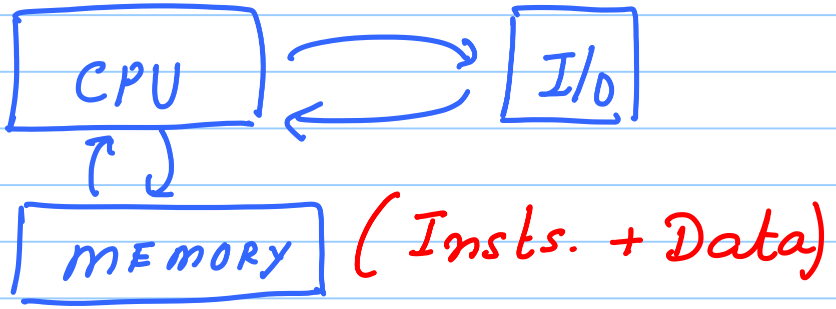
J-format

jal 25 [(pc += 4+100)
[bl] same as bl]

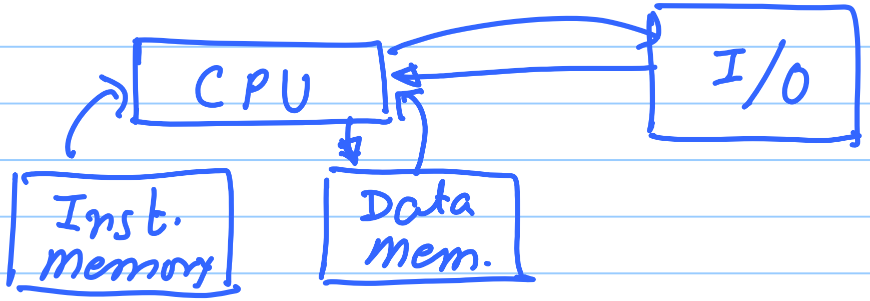
6	26
opcode	offset

Machine.

Von-neumann Machine



Harvard Machine


CPU
I/O
Inst. memory
Data mem.