Note Title 01-11-2011

Nov - 1st

Multiprocessors.

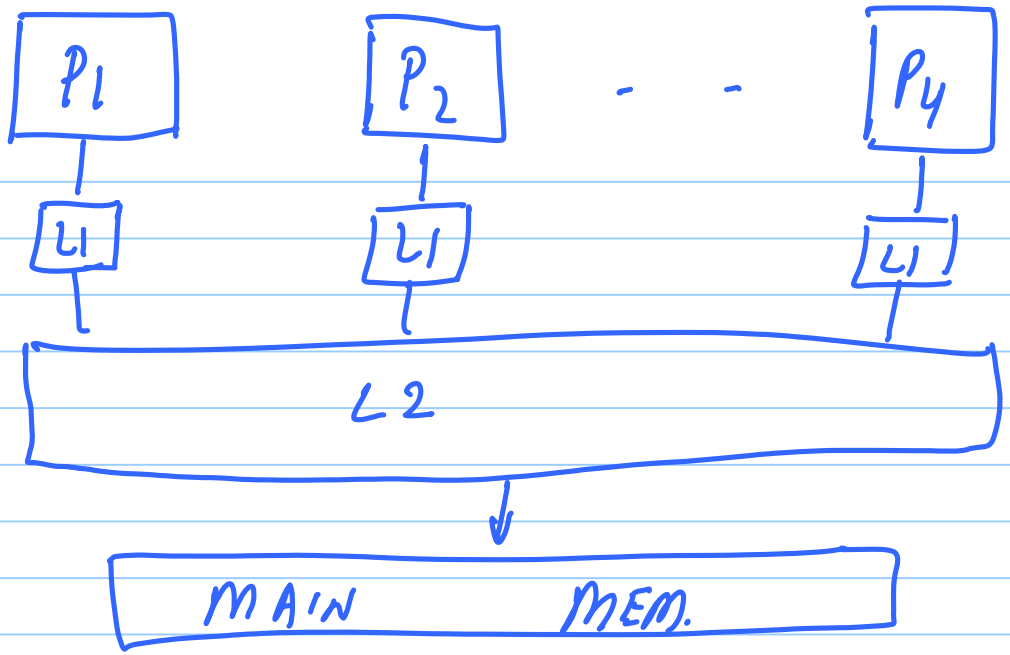
L1, L2 Mem. Lat

WB 200 cyc.

Branch Predictor: Weakly Taken.

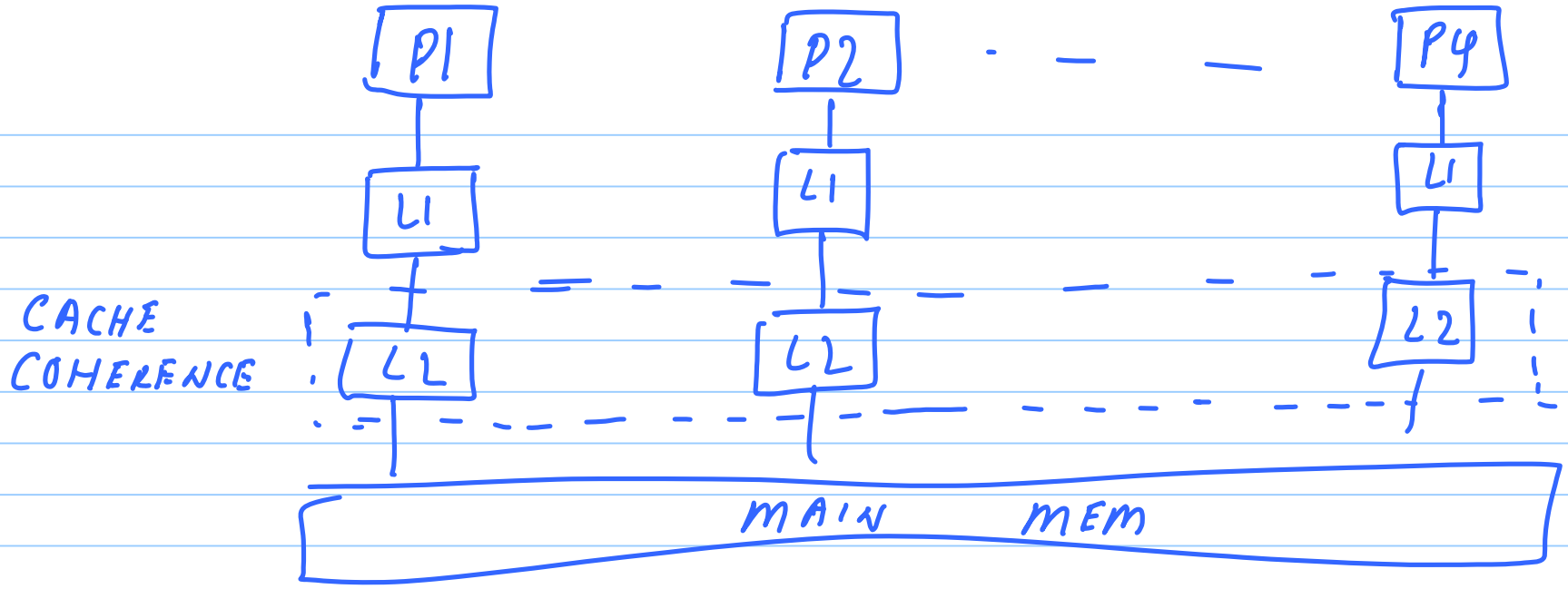
Size of switcher.

- Chip → Multiprocessor
  - → Multithreading.



UNIFIED L2

UMA
(UNIFORM - MEMORY
ARCHITECTURE)



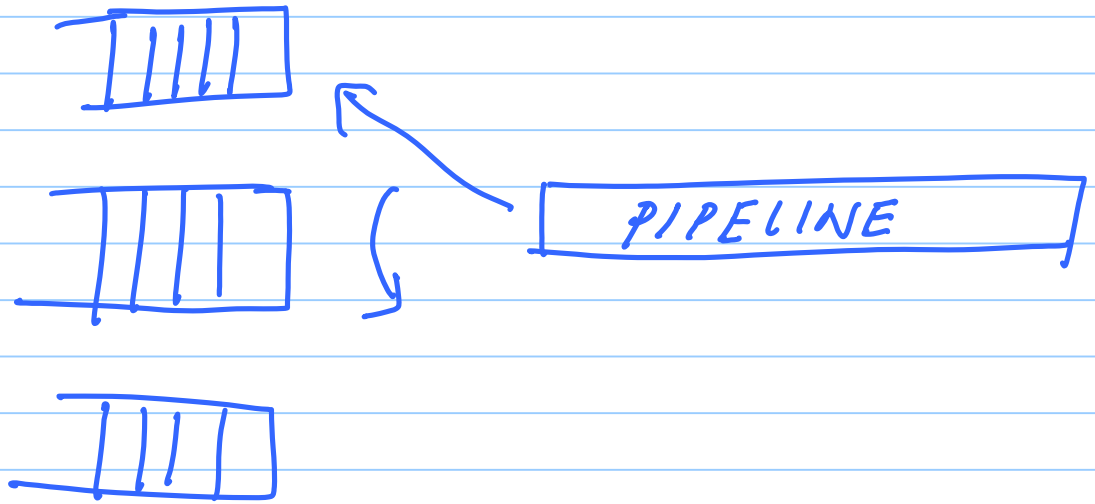
NON-UNIFORM MEMORY

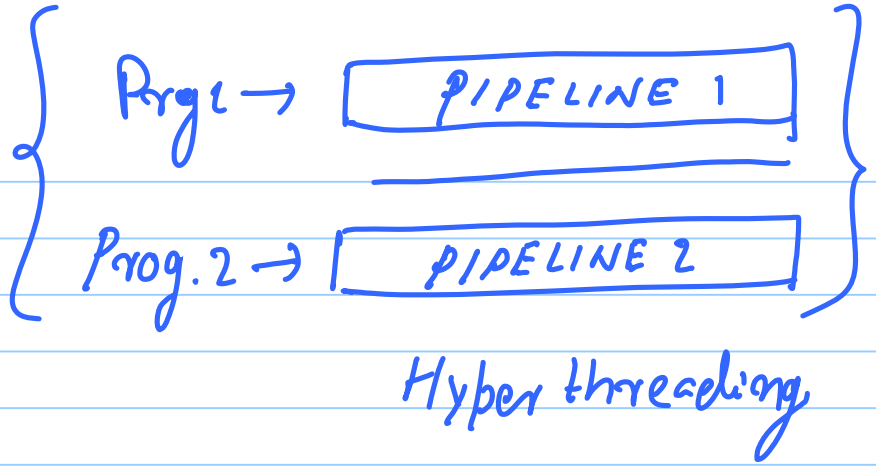
ARCHITECTURE

(NUMA)

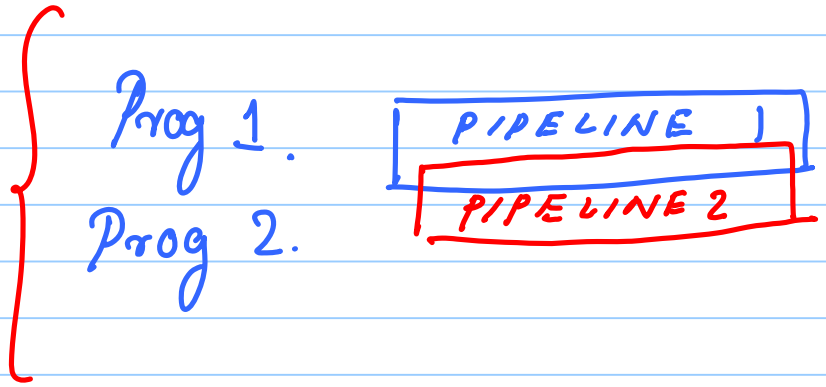
MULTI-THREADING

COARSE-GRAIN, FINE GRAIN, SIMULTANEOUS.





Hyper threading



Flynn's Classification.

S → Single

M → Multiple.

I → Instruction

D → Data.

SISD	MISD	SIMD	MIMD
Regular Sequential Program.	rare	GRAPHICS PROC. VECTOR PROC.	Normal Data.

Vector Processors

A [1 - - - 127]

B [1 - - - 127]

C [1 - — 127]

C = A + B (Vector Instr.).

Vector extensions in X86 processors:

MMX, SSE (I - IV)

Cache Coherence

Split L2 → Unified L2

Memory Consistency

A = 0 B = 0

P1	P2
A = 1	read B
B = 1	read A

B = 1

A = 1

Is the outcome

B = 1

A = 0

possible?