Shubhankar Suman Singh

Personal Data

Address: 407 A, Sector 7, Ukkunagaram, Visakhapatnam, India - 530032
Phone: +91 9990464648
Email: shubhankar039@gmail.com

Jobs

2021 - 2023	Research Scientist (Unstructured Data Storage Lab) Huawei Technology India Private Limited (HTIPL) Project: Leveraging SmartNICs and Computational Storage Devices for file system optimization.

Education

2016 - 2023	PhD in Computer Science and Engineering Indian Institute of Technology, Delhi Recipient of Prime Minister Research Fellowship (PMRF) Supervisor: Prof. Smruti R. Sarangi CGPA: 9.857/10
2012 - 2016	B.tech. in Computer Science and Engineering Indian Institute of Technology, Delhi CGPA: 9.457/10
2010 - 2012	Class XII at Mahathi Junior College, Visakhapatnam Board of Intermediate Education, Andhra Pradesh, India Final Marks: 95.8%
2009 - 2010	Class X at Delhi Public School, Ukkunagaram, Visakhapatnam Central Board of Secondary Education, CBSE CGPA: 9.8/10

Scholarships and Certificates

IIT-D Merit Award	Scholarship for top 7 percentile students in the department Awarded Silver Medal for achieving highest CGPA in the first semester Received certificate and cash prize in five semesters
Competitive Exams	Secured 217^{th} rank in Graduate Aptitude Test in Engineering (GATE-CS) Secured 125^{th} rank in IIT - Joint Engineering Examination (IIT-JEE) Secured 22^{nd} rank in All India Engineering Entrance Examination(AIEEE)

Key Skills

- **Programming Languages:** Python, Java, C, C++, VHDL.
- **Operating Systems (kernel coding):** Linux, FreeBSD, and OpenBSD.
- **Computer Architecture:** In-order and Out of Order pipelines, LSQ, TLB, Branch Predictors, Caches, ROB and NOC. **Instruction Set Architectures:** x86, RISC-V and ARM.
- **Full-system Emulators and Simulators:** Gem5, Tejas, Qemu, Pin and Spike.
- **Others:** SpaCy (NLP), Graph theory, Probability theory, Linear Algebra and Optimization.

Publications

- Shubhankar Suman Singh and Smruti R. Sarangi, *CP3: A Fast and Accurate Tool For Cross-Platform Performance Prediction*, Under review 2022.
- Shubhankar Suman Singh and Smruti R. Sarangi, *ISAMod: A Tool for Designing ASIPs by Comparing Different ISAs*, VLSI Design, 2021.
- Shubhankar Suman Singh and Smruti R. Sarangi, *ISAMon: A Tool for Cross-Platform Performance Estimation and Clone Detection Using a Novel FFT-based Code Signature*, Design Automation Conference (DAC), 2020, accepted as a poster.
- Shubhankar Suman Singh and Smruti R. Sarangi, *SoftMon: A Tool to Compare Similar Open-source Software from a Performance Perspective*, Proceedings of the 17th International Conference on Mining Software Repositories, 2020.
- Priyanka Singla, Shubhankar Suman Singh and Smruti R. Sarangi, *FlexiCheck: An Adaptive Checkpointing Architecture for Energy Harvesting Devices*, Design, Automation & Test in Europe Conference & Exhibition (DATE) 2019, 546-551.
- Priyanka Singla, Shubhankar Suman Singh, K Gopinath and Smruti R. Sarangi, *Probabilistic Sequential Consistency in Social Networks* , IEEE 25th International Conference on High Performance Computing, 2018.
- Balaji Vasan Srinivasan, Tanya Goyal, Varun Syal, Shubhankar Suman Singh, and Vineet Sharma. *Environment Specific Content Rendering and Transformation*. In Companion Publication of the 21st International Conference on Intelligent User Interfaces (IUI '16 Companion) 2016. ACM, New York, NY, USA, 18-22.
- Happy Mittal, Shubhankar Singh, Vibhav Gogate and Parag Singla. *Fine Grained Weight Learning in Markov Logic Networks*, International Workshop on Statistical Relational AI, 2016.

Patents

- Shubhankar Suman Singh and Smruti R. Sarangi, *A System and method for comparing Instruction set architecture (ISAs) for designing application specific instruction set processor*.
- Balaji Vasan Srinivasan, Vineet Sharma, Varun Syal, Tanya Goyal, Shubhankar Suman Singh, Cedric Huesler, *Content to layout template mapping and transformation*.

Talks

- TensorStore Middleware - Making storage APP aware, Huawei Scientist Workshop'22.
- Accelerating File-System operations using Computational Storage Devices, Huawei Scientist Workshop - 2022.

Work Experience

Leveraging SmartNICs and NVM for file-system optimization. JAN 2021 - PRESENT

Supervisor - Prof. Jialin Li, Computer Science Department, National University of Singapore

In this work, we propose a high-perfomance client-server filesystem, utilising SmartNICs based on Field Programmable Gate Arrays (FPGAs) and NVM-enabled SSD (Intel Optane DC SSD) to cut access latency.

- We aim at designing a low-latency metadata server on a SmartNIC (FPGA + NVM).
- Our client-server Distributed File System is managed by a cluster of metadata servers.
- The data servers are normal server nodes that have high-speed Ethernet connections.

Ph.D. Thesis

A COMPARATIVE APPROACH FOR UNDERSTANDING, ANALYZING, AND PREDICTING THE BEHAVIOR OF INSTRUCTION SET ARCHITECTURES AND OPERATING SYSTEMS

Supervisor - Prof. Smruti R. Sarangi, Computer Science Department, IIT Delhi.

PROJECT 1: INSTRUCTION SET ARCHITECTURE (ISA) COMPARISON

An automated tool to compare the performance of different ISAs: x86, RISC-V and ARM.

- A novel instruction-trace visualization to *analyze* ISA performance.
- A novel $\mathcal{FFT}$-based code signature to *estimate* ISA performance (error $< 5\%$).
- Transplant instructions from x86 to RISC-V to improve it's performance by 10%.

PROJECT 2: OPEN-SOURCE SOFTWARE AND OPERATING SYSTEMS COMPARISON

A scalable and automated tool to compare the performance of open-source software ranging from image-editors to Operating Systems ($>$ million SLOC). It has the following features:

- Extract, compress and match the execution traces of the frequent functions.
- Detect code similarity using the latest graph matching and NLP based algorithms.
- A novel graph visualization to analyze the source code for performance differences.

Exchange Program

Sakura Science Program - The University of Tokyo JUN 2017 - JULY 2017
Supervisor - Prof. Takahiro Shinagawa, Information Technology Center, UTokyo.

- The aim was to observe the lock contention due to increasing the number of cores.
- A study of different scalable lock architecture was done as part of this project.

B.Tech Thesis

FINE-GRAINED WEIGHT LEARNING IN MARKOV LOGIC NETWORK July 2015 - May 2016
Supervisor - Prof. Parag Singla, Computer Science Department, IIT Delhi.

- A framework to learn different weights for a formula in MLN depending on constraints.
- The evidence is clustered using the k-means algorithm to detect the hidden sub-types.
- Our model achieved 30% higher AUC on the IMDB dataset as compared to the baseline.

Internship

CONTENT PHYSICS ENGINE May 2015 - July 2015
Adobe Research Labs, Bengaluru.
Supervisor: Balaji Vasan Srinivasan, Senior Research Scientist, Big Data Experience Lab

- The aim of the project was to automatically distribute a *content* on a given *layout* based on its properties and also applying various transformations to the content.
- A software was developed that takes as input the various contents and a specific layout and then distributes it on the layout. We tested our model on news websites.
- The content and layout are represented as nodes in two graphs and their mapping is done based on edge weights by using the Hungarian algorithm.

Major Projects

OUT-OF-ORDER MULTI ISSUE RISC PIPELINE PROCESSOR IN VHDL JULY 2016 - NOV 2016
Supervisor - Prof. Smruti R. Sarangi, Computer Science Department, IIT Delhi

- Instruction fetch, decode, rename, window, select, ALU, commit were implemented
- Load-Store Queue, ReOrder-Buffer and Register address table were also added
- Different forwarding paths and pipeline flush were also implemented

ADDITIONS TO MULTICORE ARCHITECTURAL SIMULATOR (TEJAS) FEB 2016 - APRIL 2016
Supervisor - Prof. Smruti Ranjan Sarangi, Computer Science Department, IIT Delhi.

- Various **Branch Predictor** such as GaP, PaP, PaG, GaG were simulated.
- **Load-Store Queue** structure was added and various forwardings were simulated.
- Simulation of **NUCA, D-NUCA and R-NUCA** cache was integrated with tejas and tested on PARSEC benchmarks.