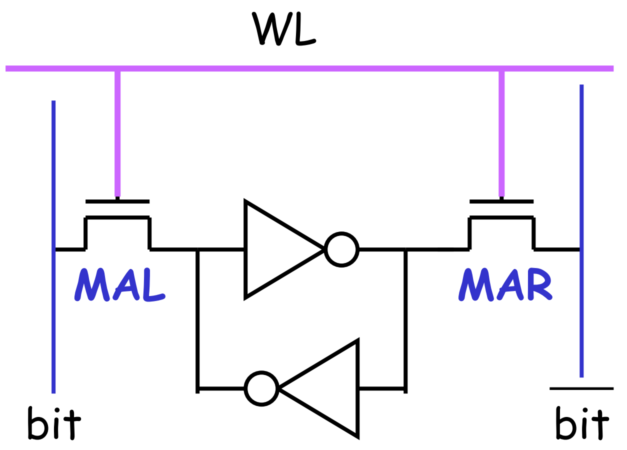
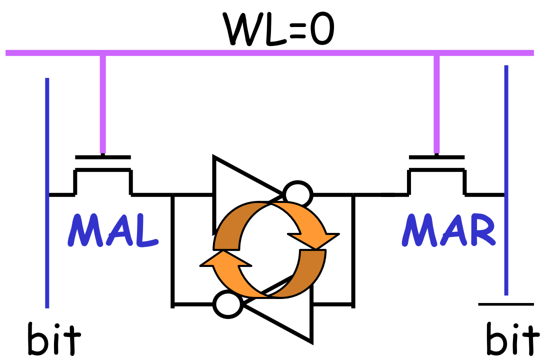
SRAM Basics

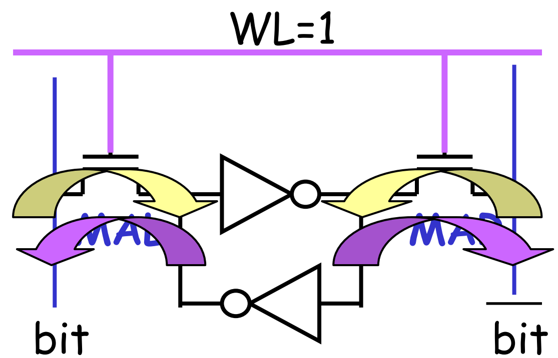
- SRAM = Static Random Access Memory
  - Static: holds data as long as power is applied
  - Volatile: can not hold data if power is removed
- 3 Operation States
  - hold
  - write
  - read
- Basic 6T (6 transistor) SRAM Cell
  - bistable (cross-coupled) INVs for storage
  - access transistors MAL & MAR
    - access to stored data for read and write
  - word line, WL, controls access
    - WL = 0, hold operation
    - WL = 1, read or write operation



SRAM Operations

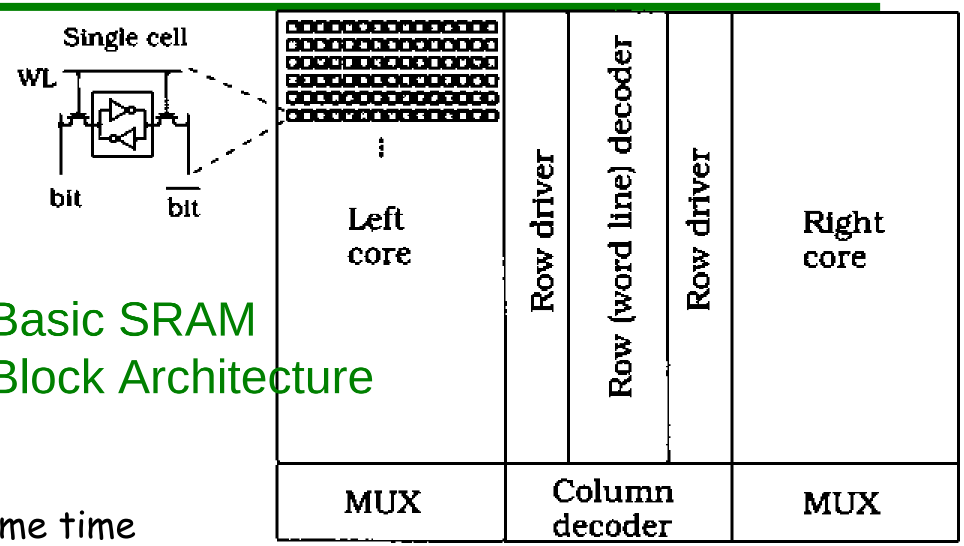
- Hold
  - word line = 0, access transistors are OFF
  - data held in latch
- Write
  - word line = 1, access tx are ON
  - new data (voltage) applied to bit and bit_bar
  - data in latch overwritten with new value
- Read
  - word line = 1, access tx are ON
  - bit and bit_bar read by a sense amplifier
- Sense Amplifier
  - basically a simple differential amplifier
  - comparing the difference between bit and bit_bar
    - if bit > bit_bar, output is 1
    - if bit < bit_bar, output is 0
    - allows output to be set quickly without fully charging/discharging bit line



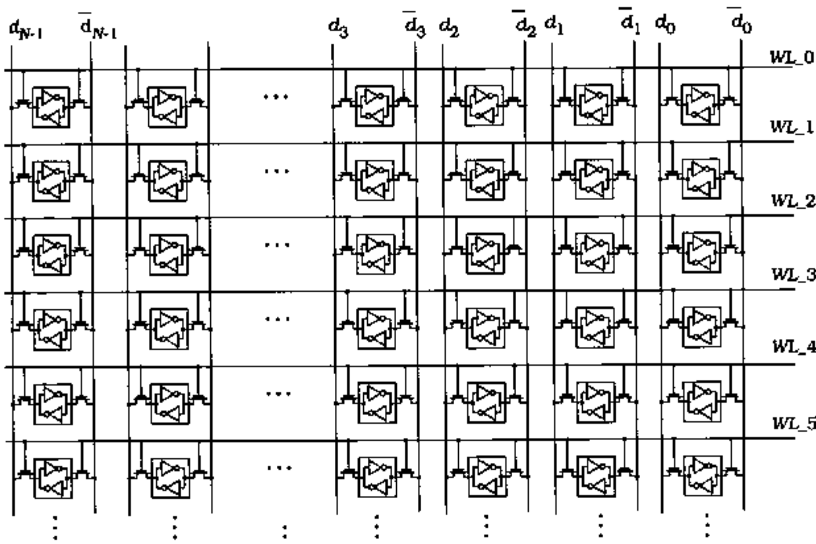


SRAM Block Architecture

- Example: 2-Core design
  - core width = k•n
    - n = SRAM word size; 8, 16, etc.
    - k = multiplier factor, 2,3,4,etc.
  - shared word-line circuits
    - horizontal word lines
    - WL set by **row decoder**
      - placed in center of 2 cores
      - WL in both cores selected at same time
- Addressing Operation
  - address word determines which row is active (which WL =1) via **row decoder**
  - row decoder outputs feed **row drivers**
    - buffers to drive large WL capacitance
- Physical Design
  - layout scheme matches regular patterning shown in schematic
    - horizontal and vertical routing



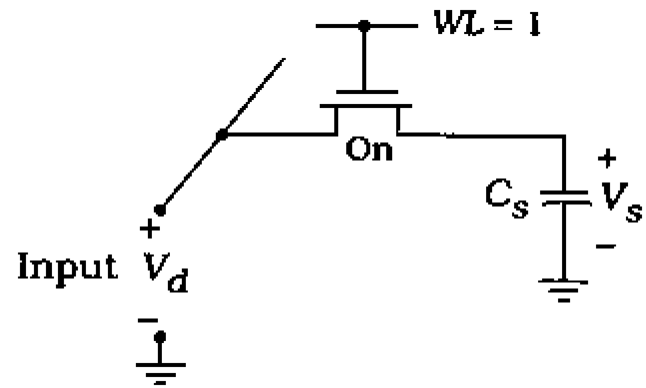
Basic SRAM Block Architecture



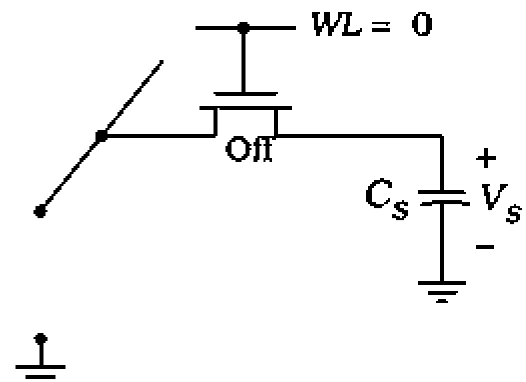
Expanded Core View

DRAM Operation

- RAM data is held on the storage capacitor
  - temporary –due to leakage currents which drain charge
- Charge Storage
  - if Cs is charged to Vs
  - Qs = Cs Vs
    - if Vs = 0, then Qs = 0: LOGIC 0
    - if Vs = large, then Qs > 0: LOGIC 1
- Write Operation
  - turn on access transistor: WL = VDD
  - apply voltage, Vd (high or low), to bit line
  - Cs is charged (or discharged)
  - if Vd = 0
    - Vs = 0, Qs = 0, store logic 0
  - if Vd = VDD
    - Vs = VDD-Vtn, Qs = Cs(VDD=Vtn), logic 1
- Hold Operation
  - turn off access transistor: WL = 0
    - charge held on Cs



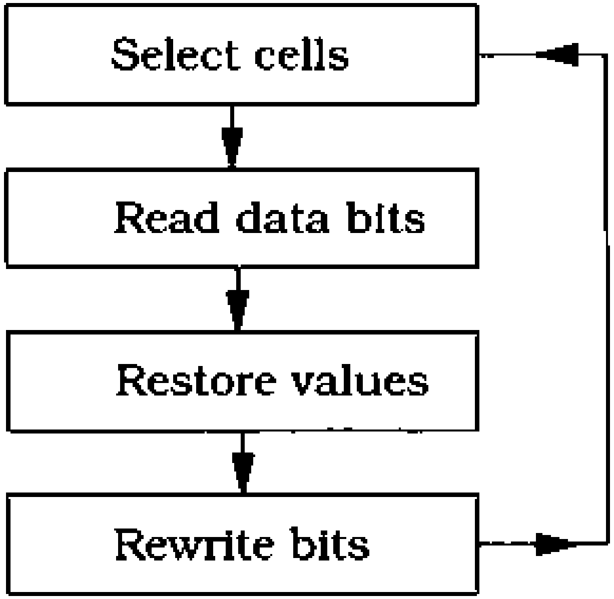
(a) Write operation



(b) Hold

Refresh Rate

- DRAM is "Dynamic", data is stored for only short time
- Refresh Operation
  - to hold data as long as power is applied, data must be refreshed
  - periodically read every cell
    - amplify cell data
    - rewrite data to cell
- Refresh Rate, $f_{refresh}$
  - frequency at which cells must be refreshed to maintain data
  - $f_{refresh} = 1 / 2t_h$
  - must include refresh circuitry in a DRAM circuit



Refresh operation

DRAM Read Operation

- Read Operation
  - turn on access transistor
  - charge on Cs is redistributed on the bit line capacitance, Cbit
  - this will change the bit line voltage, Vbit
  - which is amplified to read a 1 or 0
- Charge Redistribution
  - initial charge on Cs: Qs = Cs Vs
  - redistributed on Cbit until
    - Vbit = Vs = Vf (final voltage)
  - Qs = Cs Vf + Cbit Vf
  - Cs Vs = Vf (Cs + Cbit)
    - due to charge conservation
  - Vf = Cs Vs / (Cs + Cbit), which is always less than Vs
    - Vf typically very small and requires a good sense amplifier