

Name: _____

Roll No: _____

(COL 216) Computer Architecture

March 26, 2023

Minor 2

Duration: 60 minutes

(30 marks)

Beware: Be concise in your writing. You can use rough sheets for calculations. But you cannot submit any additional sheet for grading on Gradescope. So make sure you are certain when you write something (after rough work, or use a dark pencil). If you cheat, you will surely get an F in this course.

1. A 5-stage MIPS pipeline has a 1 cycle **load-to-use** delay i.e. you have to wait for 1 cycle between a *lw* instruction and any ALU instruction that uses it, as you cannot forward from MEM where data is ready at the end of cycle to EX where data is needed at the beginning of cycle. The pipeline is otherwise ideal i.e. the pipeline is always full, there is no forwarding delay, and each instruction takes 1 clock cycle. A program has 20% loads, but the compiler can find independent instructions to put after the load only for half of them. What is the slowdown due to delay/NOP slots? **[3 marks]**

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4. In a single cycle processor, all instructions use a common clock. The table shows the time needed by three instruction types, and their respective percentage in a set of instructions. What is the fastest clock cycle this single cycle processor can use? What percentage of time is wasted in executing 10 instructions? **[3 marks]**

Instruction	Time	% of instructions
Type 1	800 ps	30%
Type 2	200 ps	20%
Type 3	250 ps	50%

Table 1: *Instruction details*

5. A processor takes 100ns and 100pJ for every instruction. It can be infinitely pipelined with each pipeline register taking 2ns and 2pJ. What is the throughput, latency per instruction and energy per instruction for a 100 stage processor, compared to the original processor? **[3 marks]**

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6. The 5 stages of a processor have the following latencies.

Fetch	Decode	Execute	Memory	Writeback
300ps	400ps	350ps	500ps	100ps

Table 2: *Processor latencies*

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages. If you could split one of the pipeline stages into 2 equal halves, which one would you choose? Do you see any improvement in cycle time, latency for one instruction and throughput, with this split? [**4 marks**]

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7. A 1-bit saturation counter toggles between 0,1 states and a 2-bit counter toggles between 00,01,10,11 states. We build two branch predictors, one with 1-bit and the other with 2-bit counters. We have two traces of branch taken (T) and not-taken (N): Trace1: *NNNTNNN*, Trace2: *NTNTNTN*. What will be the accuracies for each trace for each predictor? Assume each counter starts at strongly not taken state. **5 marks**.

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8. What operations can the following ALU perform? Please label the diagram to describe which operation each input, gate and output in the ALU is related to? [5 marks]

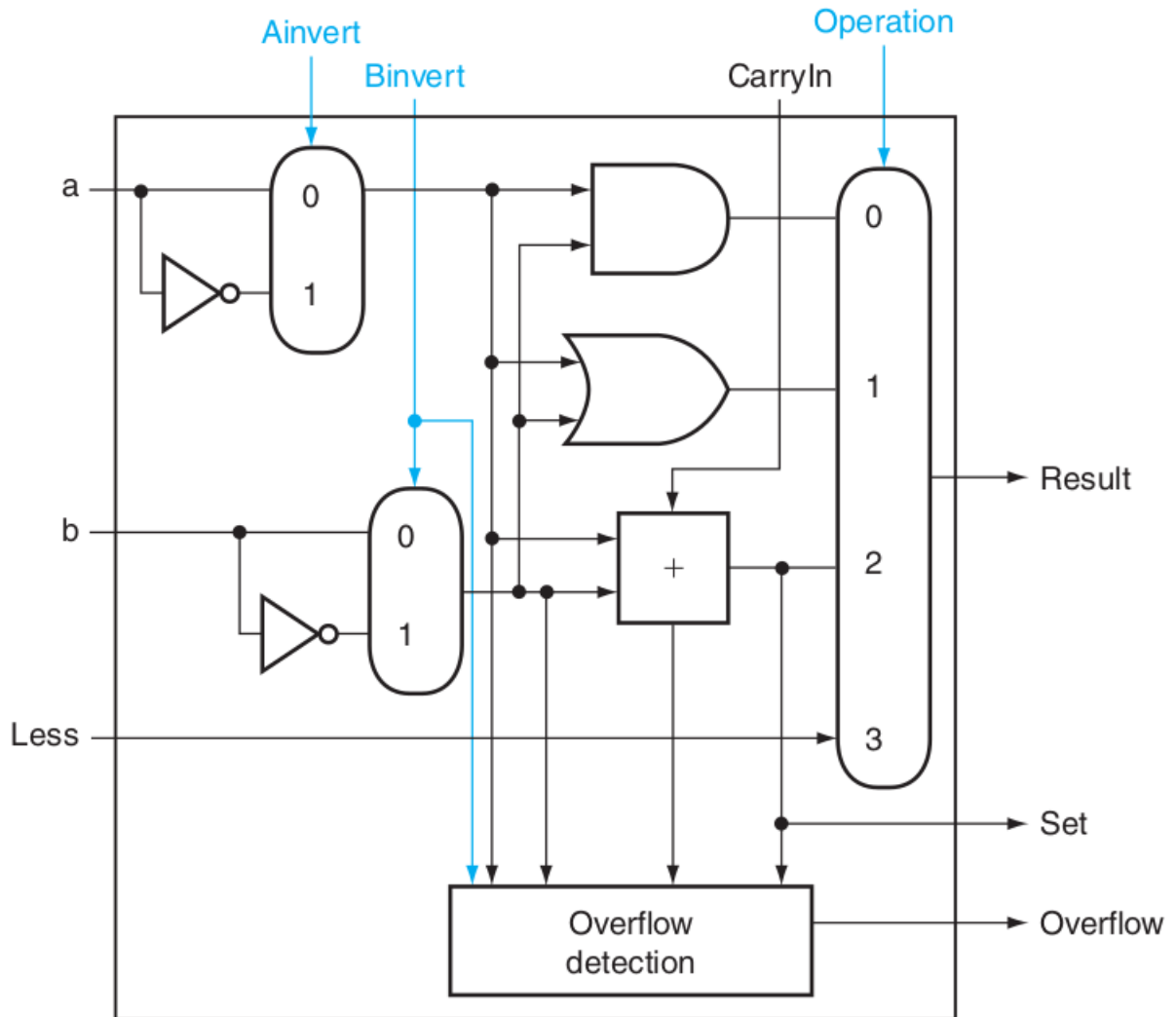


Figure 1: ALU design for arithmetic and logical operations.