Workshop on Computer Architecture Education

(http://www2.cse.iitk.ac.in/~wcae/index.html)

In conjunction with FPT 2011

The 2011 International Conference on Field-Programmable Technology

(http://www.cse.iitd.ac.in/~icfpt11/)

December 15th, 2011 - IIT, Delhi, India

Abstract Deadline: October 31, 2011

The objective of this workshop is to solicit presentations on successful experiences and promising ideas for teaching Computer Architecture and Digital Design.

Computer architecture education today is mostly descriptive and does not provide the excitement and intellectual vigor to the students that come from problem solving and hands-on design experience. Simple pipelined architectures are taught using abstract circuit diagrams depicting gates, registers and memories, while more complex architectures are taught even more informally. Is this primarily due to the non-availability of tools and design techniques that permit quick explorations of design alternatives? Can this situation be changed?

The goal of the workshop is to bring together educators and researchers who have experience in teaching computer architecture and digital design and learn from their experiences. We would like the participants to share their experiences in using the tools and techniques they use for teaching. We will have a keynote by Professor Arvind, MIT, on the novel approach to teaching architecture and digital design that he has been experimenting with at MIT and Seoul National University.

Topics of interest to the workshop include, but are not limited to:

- The use of Instruction Set Simulators
- The use of advanced simulators such as PIN and Simple Scalar
- The use of Hardware Description Languages like Verilog and VHDL
- Use of system modeling languages like SystemC
- Use of high-level synthesis languages like Bluespec
- Use of FPGA based laboratories
- News tools for designing and describing architectures and digital circuits

Target Audience:

Teachers, professors in the area of computer architecture, digital design, compilers, EDA tools etc.; practicing architects and designers. Anyone who would like to contribute to hands-on design courses.

Please submit an abstract (maximum 500 words) to karkare@iitk.ac.in. We will try to accommodate everyone who wants to speak as permitted by the time constraint.

Registration fee:

Rs. 2000.00 for Indian Academicians (students and faculty members) and Rs. 5000.00/USD 100.00 for others. The registration fee includes lunch and coffee breaks. Some sponsorship might be available for supporting the registration fee for Indian Academicians for which the participants may contact Prof. V Kamakoti (veezhi@gmail.com).

Organizers:

- Arvind Computer Science and Artificial Intelligence Lab, MIT
- M. Balakrishnan Department of CSE, IIT Delhi
- V. Kamakoti Department of CSE, IIT Madras

- Ameya Karkare Department of CSE, IIT Kanpur
- Jihong Kim Seoul National University
- Rajat Moona Department of CSE, IIT Kanpur and C-DAC

Tentative Schedule:

- Session 1 (09:00-11:30)
 - 09:00-09:30 Registration
 - 09:30-10:30 Tutorial on Architecture Course design by Prof. Arvind, MIT
 - 10:30-11:30 Invited talks by eminent Professors on their experiences in innovating education in Computer Architecture.
- Session 2 (11:45-13:30): Presentations by contributors.
- Session 3 (14:30-16:30): Discussions and experience sharing.
- Session 4 (17:00-18:30): Panel Discussion and Wrap up session.