# Reducing Clocks in Timed Automata while Preserving Bisimulation 

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## The problem we solve

Given a timed automaton (TA), is it possible to minimize the number of clocks of a timed automaton while preserving timed bisimulation?

Mentioned and left open in (LLW1 '95)

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Contribution
We give a procedure to construct a TA with the minimum possible number of clocks while preserving timed bisimulation.

## Importance

Verification and model checking of timed automata uses
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that has a size exponential in the number of the clocks.

- smaller number of clocks implies smaller region graph or zone graph and thus easier verification


## A Timed Automaton



## Semantics: Timed Labeled Transition System (TLTS)

- Infinite transition graph structure
- Nodes are timed automaton states; tuple ( $\ell, v$ )
- Two types of transitions

Discrete transitions : a Act: $(\ell, v) \xrightarrow{a}\left(\ell^{\prime}, v^{\prime}\right)$ if there is an edge $\left(\ell \xrightarrow{g, a, r} \ell^{\prime}\right) \in E$ and $v \vDash g, v^{\prime}=v[r]$

Delay transitions : $d \in \mathbb{R}_{\geq 0}:(\ell, v) \xrightarrow{d}(\ell, v+d)$.

## Timed Bisimulation

$p$ and $q$ are two timed states.


## Related Work: Clock Reduction

## Preserve timed language

- No algorithm can decide the minimality of the number of clocks and
for the non-minimal case find a timed language equivalent automaton with fewer clocks. (Tripakis '04)


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## Preserve timed language

- No algorithm can decide the minimality of the number of clocks and
for the non-minimal case find a timed language equivalent automaton with fewer clocks. (Tripakis '04)
- Existence of a language equivalent timed automaton with smaller number of clocks is also undecidable (Finkel '06)


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## Preserve timed bisimulation

- An algorithm to reduce the number of clocks is provided in (DY '96)

It works on a syntactical structure of the timed automaton and does not provide the minimum number of clocks

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## Preserve timed bisimulation

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- Checking the existence of a $(C, M)$ automaton timed bisimilar to a given TA is decidable (LLW '95).
$C$ : number of clocks and $M$ : maximum constant used in the automaton

The problem of the current paper was "left as an open (and interesting) problem". conclusion of (LLW '95)

## Our Approach

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1. Remove constraints that are never enabled (Stage 1)
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4. Multiple outgoing transitions from a location when considered collectively can remove some constraints (Stage 3)
5. An efficient renaming of clocks across all the locations of the timed automata (Stage 4)

- Input TA A : Through four stages we get $A_{4}$ which preserves timed bisimulation and $A_{4}$ has the least possible number of clocks.


## Stage 1: Construct Zone Graph

- Nodes: $(I, Z), I$ : location, $Z$ : zone.
- zone: A zone $z=\left\{v \in \mathbb{R}_{\geq 0}^{|C|} \mid v \models \gamma\right\}$, where $\gamma$ is of the form $\gamma::=x \smile c|x-y \smile c| g \wedge g$, where $c \in \mathbb{Z}, x, y \in C$ and $\smile \in\{\leq,<,=,>, \geq\}$.
- A zone is a convex set of valuations


## Prestabilizing Zones



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## Pre-stability

## An important property

Pre-stability ensures that if

- the zone $Z$ in any node $(I, Z)$ in the zone graph is bounded above,
- then it is bounded fully from above by a hyperplane $x=h$, where $x \in C$ and $h \in \mathbb{N}$.


## Stage 1: Construct Zone Graph



Consider an edge $I \xrightarrow{g, a, R} I^{\prime}$ If for all nodes $(I, Z), Z \cap \llbracket g \rrbracket=\emptyset$, then remove the edge.

## Splitting locations: Stage 2

Base zones: Zones without delay predecessors


Some constraints removed from the newly created locations and clocks can be reused

## Splitting locations: Stage 2

Base zones: Zones without delay predecessors


Number of newly created locations bounded by the number of zones: hence exponential in the number of clocks

No change in underlying semantics; zones distributed to different locations, hence $A_{2}$ timed bisimilar to $A$.

## Remove constraints by considering multiple outgoing edges: Stage 3



Multiple outgoing edges from the same location
Consider zones with the same set of actions enabled.
Check if removing some hyperplanes and hence some constraints from the zone graph preserves timed bisimilarity.

## Remove constraints by considering multiple outgoing edges: Stage 3



Check if removing hyperplanes and thus merging some zones preserves timed bisimilarity.

Timed bisimilarity can be checked using the zone graph. (LZ '97, GKNA '13)

## Remove constraints by considering multiple outgoing edges: Stage 3



Removing constraints can lead to a reduction in the number of clocks.

Since every constraint removal checks timed bisimulation explicitly, $A_{3}$ is timed bisimilar to $A$.

## Clock renaming: Stage 4

Finding active clocks
Active clocks (act(/)) : clocks whose valuations are relevant for defining the behaviour of the timed automaton from location $/$.

$\operatorname{act}\left(l_{0}\right)=\left\{x_{0}, y_{0}\right\}, \operatorname{act}\left(l_{1_{1}}\right)=\left\{y_{1_{1}}\right\}, \operatorname{act}\left(l_{1_{2}}\right)=\left\{x_{1_{2}}\right\}, \operatorname{act}\left(I_{1_{3}}\right)=$ $\left\{x_{1_{3}}\right\}, \operatorname{act}\left(l_{2}\right)=\emptyset$.

## Clock renaming: Stage 4

## Partitioning active clocks

Active clocks: Partition act(I) at a location I into equivalence classes.
$\forall x, y \in \operatorname{act}(I), x \equiv y$ iff $\exists c \in \mathbb{N} . x-y=c$.
E.g. $x_{0}-y_{0}=0$.


## Clock renaming: Stage 4

Vertex colouring of the clock graph


This graph can be coloured using one color.

## Complexity: Stage 4

- Number of vertices in clock graph:
- Bounded by the number of locations $\times$ number of clocks,
- Hence, exponential in the number of clocks
- Graph colouring: EXPTIME in the number of vertices
- Thus, 2 - EXPTIME in the number of the clocks.


## Minimality of clocks

Semantically every hyperplane in the zone graph of $A_{4}$ indicates a change in the behaviour and is essential for preserving bisimulation.

## Minimality of clocks

Minimal bisimilar TA
For a given timed automaton $D$, a minimal bisimilar TA is one that is

- timed bisimilar to $D$ and
- has the minimum number of clocks possible.

Fact
For every TA D, there exists a minimal bisimilar TA.
The timed automaton $A_{4}$ has the same number of clocks as a minimal bisimilar TA for $A$.

## Our Result

## Theorem <br> Given a timed automaton $A$,

- there exists an algorithm to construct a TA $A_{4}$
that is timed bisimilar to $A$ such that
- among all the timed automata that are timed bisimilar to $A$
- $A_{4}$ has the minimum number of clocks.
- Further the algorithm runs in time that is doubly exponential in the number of clocks of $A$.


## Questions

