Project Report

Message Display Module

Supervisor:  
Prof. M. Balakrishan

Project Members:  
Harshal Bidasaria (2010CS50283)  
Shantanu  (2010CS50295)  
Utkarsh  (2010CS50299)
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**Introduction:**

This report has been written to describe the functional as well as operational details of Message Display Module developed as part of final project for Digital Hardware Design course (CSL316) under the supervision of Professor M. Balakrishnan. This document describes the various components used in realizing the design, the purpose of using those components, the finite state machine depicting how the module operates. This document also specifies the various interfaces which link the sub modules.

Message display find their use in various service related applications. For example in advertisement sector, displaying important announcements in restaurants, hospitals etc. Every module is customised for the application it is used. Some display blinking texts (for displaying warning signs), some display lists (news bulletin) etc.

In our message display module, we have displayed a string undergoing a marquee behaviour. The aim of developing this module is to learn about how interfacing of LCDs is done.
**Project Design:**

**Components Used:**

- Spartan 6 FPGA (Digilent Atlys)
- 16x2 LCD Unit (CP162A)
- USB UART for communication between FPGA and PC
- Pmod Expansion port for communication between LCD and FPGA
- PuTTY/TeraTerm terminal client for sending commands to the board
- Set of ICs (2x 74HC125) and bread board to set up level shifter circuit (convert 3.3V signals to 5.0V signals)
- 5.0V Voltage source for LCD operation.

**Design Description:**

The main components of the design include the PC, FPGA, Aux Circuit (ICs and bread board forming the level shifter circuit) and the LCD sub module. The PC communicates with the FPGA through a terminal based client over USB-UART connection. The FPGA communicates with the LCD sub module through the PMOD expansion port on the Spartan-6 board. Following is the description of the individual modules:

**PC:** At the PC, a terminal based client (PuTTY) is spawned in order to establish serial communication over a COM port which is masked on USB ports. The BAUD rate and the frame configuration of the link needs to be configured. (8 data bits, 1 start bit, 1 stop bit, no parity and 2400bps baud rate).

**FPGA:** The FPGA has been programmed as a micro blaze processor using Xilinx Platform Tools and the program for displaying message has been developed using the Xilinx Software Development Kit. The PMOD expansion port of the
FPGA are used for interfacing the LCD with the FPGA. We use 4 data bits, 1 bit for R/W, 1 bit for enable (pulse trigger).

**Aux Circuit:** A potential problem in operation of LCD submodule was that it needed signals which operated at minimum 4.2V, and the voltage at which the dicipent board operated was 3.3V. Hence the signals generated by the FPGA were not able to drive the LCD. So this auxiliary circuit was built. It takes the 6 signals from the FPGA submodule, steps up the voltage level and feeds the output 6 signals to the LCD submodule.

**LCD Module:** The LCD submodule we have is 16x2 CP162A. The module operates in two modes (4-bit and 8-bit). Since we were using 4 data bits, we use the LCD in 4-bit mode. Since we are only writing data to LCD memory we have grounded the R/W bit (0 for Write) This is realized by sending certain command signals to the LCD submodule when it powered on and initialized. This is followed by a series of commands for clearing the display and initializing the position of the cursor on the LCD. Delay is added between successive commands for stable operation of LCD. The LCD displays the message supplied as input in a marquee fashion. In addition to all of the above, a variable resistance is needed in order to change the contrast of the LCD.

**FSM Operation:**

![FSM Diagram]

The above FSM describes the operation of the message display module. State 0 is the initial state which waits for input. Once the input is sent from the PC through the terminal, the LCD displays the input string. The string appears to shift from left to right (marquee behaviour). Now if the user presses the reset button, the module transits to State 0 and the module waits for input.
**Protocols for Using the Message Display Module:**

- Constant 5V input voltage to auxiliary circuit (bread board)
- Constant 3.3V input voltage to the FPGA (Digilent board)
- PuTTY/ TeraTerm terminal client
- USB-UART drivers for PC OS for the Spartan-6 board
- UART configuration: 8 data bits, 1 stop bit, 1 start bit, no parity
- UART configuration: Baud Rate: 2400bps

**Scenarios where the design might not work:**

- The level shifter circuit isn’t supplying constant 5V output
- The FPGA is not supplying consistent output signals (clock, user constraints configuration)
- The Baud rate is not 2400bps
- The UART frame has not been configured correctly
- The COM port on PC doesn’t match the port on which the user wants terminal to send messages to the FPGA

**Possible Feature Additions:**

- Extending module for large LCDs
- Adding memory to the module for displaying multiple messages
- Displaying text in blinking form rather than marquee behaviour
- Extending programming interface for Module so that it can be linked to multiple sources and not just one PC
- Extending communication interface from USB UART to Ethernet/Wi-Fi to support above mentioned extension
- Adding logic for controlling duration of displayed message. The duration could be customizable or function of number of messages in the memory that need to be displayed
Screenshots of Module:
References:

- [http://www.microchip.com/forums/m742506.aspx](http://www.microchip.com/forums/m742506.aspx)
- Datasheet CP162A LCD Module